WAVE DIGITAL MODEL OF THE MXR PHASE 90 BASED ON A TIME-VARYING RESISTOR APPROXIMATION OF JFET ELEMENTS

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ABSTRACT

Virtual Analog (VA) modeling is the practice of digitally emulating analog audio gear. Over the past few years, with the purpose of recreating the alleged distinctive sound of audio equipment and musicians, many different guitar pedals have been emulated by means of the VA paradigm but little attention has been given to phasers. Phasers process the spectrum of the input signal with time-varying notches by means of shifting stages typically realized with a network of transistors, whose nonlinear equations are, in general, demanding to be solved. In this paper, we take as a reference the famous MXR Phase 90 guitar pedal, and we propose an efficient time-varying model of its Junction Field-Effect Transistors (JFETs) based on a channel resistance approximation. We then employ such a model in the Wave Digital domain to emulate in real-time the guitar pedal, obtaining an implementation characterized by low computational cost and good accuracy.

1. INTRODUCTION

The advent of Digital Audio Effects (DAFx) disrupted the way in which music was conceived, recorded, and played. Nonetheless, many musicians were – and still are today – interested in using and recreating the sound of analog equipment or of a particular effect chain. Hence, Virtual Analog (VA) modeling rose as a way to reproduce that particular *analog feel* in the digital domain, such that musicians could continue to take advantage of their beloved audio effects [1].

Through the years, two main approaches have been followed for developing VA algorithms: (i) *white-box* methods, which rely on prior knowledge of the physics of the device, typically by solving systems of ordinary differential (or algebraic) equations, e.g., underlying the circuit network, using Port-Hamiltonian methods [2], state-space methods [3] or Wave Digital Filters (WDFs) [4]; (ii) *black-box* methods, which leverage on input-output measurements using, e.g., Wiener-Hammerstein models [5], Volterra series [6], or machine learning [7]. Some algorithms can be also classified as *grey-box* methods as they do use prior knowledge of the reference systems and, at the same time, differentiable models optimized by means of measurement data [8].

Until a few years ago, most of the research in VA modeling was about distortion [9, 10], fuzz [5], reverb and delay [11] effects and just little attention was given to modulation effects, such as flangers and phasers. Modulation effects, typically obtained thanks to some sort of Low-Frequency Oscillators (LFOs), are hard to model due to their intrinsic nonlinearities and time-varying nature [12]. In particular, the phasing effect introduces time-varying notches in the spectrum of the input signal, realized via all-pass filters [13]. Indeed, phasers are commonly realized as a cascade of F all-pass filters (usually, with $F \bmod 2 = 0$) whose break frequency, modulated by an LFO, determines the location of the $F/2$ notches. One of the first works about digital implementations of phasers can be found in [12], where the author provided a general model for analog reference pedals with particular emphasis on phase-shifting stages. In [14], the nodal DK method [15] is employed to derive a physical model of the famous phaser MXR Phase 90. A grey-box model is, instead, proposed in [13], where the authors use a series of short chirps for measuring the characteristics of a linear time-variant system with the aim of approximating the temporal behavior of the pedal. Finally, in [8], a differentiable signal processing approach was considered for training a model able to emulate an analog phaser circuit while retaining interpretable parameters. The literature is thus geared towards black-/grey-box models for addressing such effects, lacking still further contributions as far as white-box models are concerned.

In this work, we propose a novel and lightweight white-box model of the MXR Phase 90 guitar pedal. The core of such an effect is the chain of four phase-shifting stages, whose filters are modulated thanks to a Junction Field-Effect Transistor (JFET) driven by an LFO. Thus, the circuit presents multiple multi-port nonlinearities which make the digital emulation particularly demanding. However, the role of JFETs in this circuit is not that of amplifiers but rather of time-varying resistors, which allow the notch to shift in time. Thus, similarly to what proposed in [16], we here present a time-varying resistor approximation of such transistors by taking into account their current-voltage characteristic equations. Indeed, the use of time-varying resistors for approximating nonlinear elements goes back a long way and sees different contributions in the literature [17, 18, 16]. Then, we test the proposed model using WDFs, i.e., a particular class of digital filters that were introduced in the late '70s by A. Fettweis for digitizing lumped passive electrical filters [4]. Thanks to their intrinsic modularity and the separation between topology and element description, WDFs are well suited to VA modeling applications as they are typically characterized by a low computational cost. In fact, unlike what is typically possible to accomplish with other techniques, WDFs are able to describe circuits with up to one nonlinear one-port [19] or multi-port element [9] (characterized by an explicit mapping in the Wave Digital domain) without resorting to any iterative solver, obtaining thus remarkably cost-effective representations. Moreover, WDFs turned out to be highly efficient even

in presence of multiple one-port nonlinear elements when iterative solvers (e.g., fixed-point [20] or Newton-Raphson [21] methods) must be considered, also thanks to their intrinsic possibility to build parallel algorithms [22]. For instance, such digital filters were used to emulate vacuum tubes [23, 24, 25], waveshapers [10], ring modulators [20], distortion pedals [9], but to the best of our knowledge, they were never employed to emulate phasers. In the light of these considerations, we here realize the proposed model in the Wave Digital (WD) domain, obtaining an implementation characterized at the same time by good accuracy, real-time capability, as well as physical interpretability. It is worth pointing out that, with respect to the JFET model proposed in [16], our model is realized as a WD one-port block instead of a three-port block, allowing for a direct connection to a single topological junction without creating Delay-Free Loops (DFLs). Finally, a real-time plug-in is realized using the JUCE framework [26] to demonstrate the applicability of the proposed physical model.

The manuscript is organized as follows. Section 2 provides background on WDFs, Section 3 delves into the different stages constituting the MXR Phase 90 schematic, while the time-varying resistor approximation is proposed in Section 4, both in Kirchhoff and WD domains. The WD digital implementation of the guitar pedal is shown in Section 5, whereas conclusions are drawn in Section 6.

2. BACKGROUND ON WDFS

Let us introduce important concepts of the WDF theory, which will be fundamental later on for presenting the proposed MXR Phase 90 model. The design of WDFs starts from the port-wise description of the reference circuit [4, 27]; the port voltage v and port current i (the so-called Kirchhoff variables) are turned into an incident wave a and a reflected wave b by means of a particular wave mapping. Although many different mappings are available in the literature [4, 28, 29, 30], here we consider just voltage waves, as they are the most widespread. Such a linear transformation from Kirchhoff variables to wave variables can be written as [4]

$$a = v + Zi\,, \qquad b = v - Zi\,, \tag{1}$$

where Z is a free parameter called *port resistance* that constitutes an important degree of freedom in the Wave Digital (WD) representation [4].

Topology and elements are described in a separate fashion by means of input-output blocks characterized by scattering equations. When two WD blocks are connected together, DFLs are formed due to the instantaneous dependence between incident and reflected waves [4]. Nonetheless, by properly setting the port resistance, it is possible to remove such an implicit relation. In this case, the element or the port of the junction where the DFL is broken is said to be *adapted*. It is worth pointing out that *port adaptation* is usually possible only for linear elements and, thus, nonlinear elements must be treated differently [20].

2.1. Modeling Linear Elements

In [27], it is shown that all the common linear one-port elements (including dynamic elements such as inductors and capacitors) can be represented in the WD domain by means of a Thévenin equivalent. In fact, starting from the equation describing the discrete-time Thévenin equivalent in the Kirchhoff domain

$$v[k] = R_\mathrm{e}[k]i[k] + V_\mathrm{e}[k]\,, \tag{2}$$

where k is the sample index and $R_\mathrm{e}[k]$ and $V_\mathrm{e}[k]$ are resistive and voltage parameters, and applying (1), it is possible to obtain the WD Thévenin equivalent as

$$b[k] = \frac{R_\mathrm{e}[k] - Z[k]}{R_\mathrm{e}[k] + Z[k]}a[k] + \frac{2Z[k]}{R_\mathrm{e}[k] + Z[k]}V_\mathrm{e}[k]\,. \tag{3}$$

According to the particular element to be modeled, $R_\mathrm{e}[k]$ and $V_\mathrm{e}[k]$ assume different values and expressions [27]. The instantaneous relation between b and a in (3) can be removed by setting $Z[k] = R_\mathrm{e}[k]$; in this case, (3) becomes just $b[k] = V_\mathrm{e}[k]$ and the element is said to be *adapted*.

Linear multi-port elements can be, instead, efficiently realized employing *vector waves*. The interested reader is referred to [30] for gaining a clear understanding of the method.

2.2. Modeling Connection Networks

Topological junctions (or connection networks) are modeled as N-port WD blocks. The scattering equation is now in the form $\mathbf{a} = \mathbf{S}\mathbf{b}$ [4], where $\mathbf{S}$ is the so-called scattering matrix, $\mathbf{a} = [a_1, \ldots, a_N]^\mathrm{T}$ is the vector of waves incident to the elements and reflected by the junction, and $\mathbf{b} = [b_1, \ldots, b_N]^\mathrm{T}$ is the vector of waves reflected by the elements and incident to the junction. Matrix $\mathbf{S}$ can be obtained from the very same loop or cut-set analyses typically done in the Kirchhoff domain by considering one of the two equivalent formulas [31, 29]

$$\mathbf{S} = 2\mathbf{Q}^\mathrm{T}(\mathbf{Q}\mathbf{Z}^{-1}\mathbf{Q}^\mathrm{T})^{-1}\mathbf{Q}\mathbf{Z}^{-1} - \mathbf{I}\,, \tag{4}$$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}^\mathrm{T}(\mathbf{B}\mathbf{Z}\mathbf{B}^\mathrm{T})^{-1}\mathbf{B}\,, \tag{5}$$

with $\mathbf{I}$ being the $N \times N$ identity matrix, and $\mathbf{Q}$ and $\mathbf{B}$ being the fundamental cut-set and loop matrices, respectively. Moreover, $\mathbf{Z}$ is a diagonal matrix having on the main diagonal the vector of port resistances $[Z_1, \ldots, Z_N]$.

Finally, if operational amplifiers (opamps) are present in the circuit schematic, we can substitute them with their *nullor-based model*, which, in turn, can be encompassed into connection networks [10]. This holds true only if we consider the opamp to be ideal. From the resulting connection network, we can then derive the so-called V-net and I-net which allow us to obtain the scattering matrix describing the overall topology with [10]

$$\mathbf{S} = 2\mathbf{Q}_\mathrm{V}{}^\mathrm{T}(\mathbf{Q}_\mathrm{I}\mathbf{Z}^{-1}\mathbf{Q}_\mathrm{V}{}^\mathrm{T})^{-1}\mathbf{Q}_\mathrm{I}\mathbf{Z}^{-1} - \mathbf{I}\,, \tag{6}$$

$$\mathbf{S} = \mathbf{I} - 2\mathbf{Z}\mathbf{B}_\mathrm{I}{}^\mathrm{T}(\mathbf{B}_\mathrm{V}\mathbf{Z}\mathbf{B}_\mathrm{I}{}^\mathrm{T})^{-1}\mathbf{B}_\mathrm{V}\,, \tag{7}$$

where $\mathbf{Q}_\mathrm{V}$ and $\mathbf{Q}_\mathrm{I}$ are the fundamental cut-set matrices of the V-net and I-net, whereas $\mathbf{B}_\mathrm{V}$ and $\mathbf{B}_\mathrm{I}$ are the fundamental loop matrices of the V-net and I-net, respectively.

3. ANALYSIS OF THE MXR PHASE 90

In this section, we briefly describe the stages that compose the MXR Phase 90 schematic but the power supply and the LFO stages. These are modeled through common digital signal processing techniques as they are deemed sufficient for reaching the overall goal. The reference schematic is available at `electrosmash.com/mxr-phase90`.

Input Buffer Stage: Fig. 1 shows the schematic of the input stage. It is a simple buffer stage realized by means of an opamp and features an RC network that filters out the humming noise. The output V_1 of the opamp is then fed as input to the next stage, i.e.,

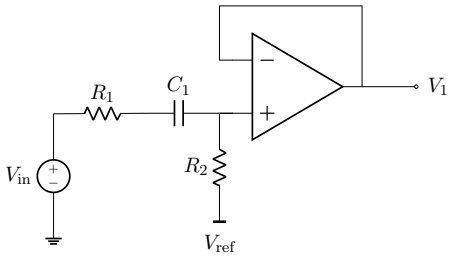

Figure 1: *Schematic of the MXR Phase 90 input stage.*

the phase-shifting stage. The parameter values are the following: $R_1 = 10$ kΩ, $C_1 = 0.01$ µF, $R_2 = 470$ kΩ, and $V_{\text{ref}} = 5.1$ V.

Phase-Shifting Stage: Fig. 2(a) shows the schematic of a single phase-shifting unit. This is the circuital realization of a first-order all-pass filter that, once expressed in the Z-domain, implements the following transfer function

$$A(z) = \frac{c_1 + z^{-1}}{1 + c_1 z^{-1}}\,, \tag{8}$$

where the coefficient c_1 can be expressed as a function of the break frequency ω_{b} of the filter (in rad/s) as [13]

$$c_1 = -\frac{1 - \tan(\omega_{\text{b}} T_{\text{s}}/2)}{1 + \tan(\omega_{\text{b}} T_{\text{s}}/2)} \approx -1 + \omega_{\text{b}} T_{\text{s}}\,, \tag{9}$$

with T_{s} being the sampling frequency. Such a filter changes nothing but the phase response of the system. In addition, we can express the break frequency as a function of the circuit parameters and the desired phase shift ϕ_{ss} as follows [14]

$$\omega_{\text{b}} = \frac{\tan\left(\phi_{\text{ss}}/2\right)}{\left(R_5 \parallel R_{\text{JFET}}\right) C_2}\,, \tag{10}$$

where R_{JFET} is the drain-source resistance of JFET Q_1. In particular, at ω_{b} such a filter introduces a phase shift of $-\pi/2$; moreover, when multiple filters are cascaded, the overall phase response is the sum of the single phase responses. Hence, being F the number of first-order all-pass filters in the cascade, the maximum phase-shift that can be introduced is $-F\pi$ [13]; for the considered phaser pedal, $F = 4$ holds true. It is worth pointing out that, in this work, we aim at modeling the first version of the MXR Phase 90, i.e., the one that dates back to 1974. With respect to modern editions, the first lacks a feedback resistor (or potentiometer) that connects the negative terminal of the second unit opamp to the output of the last unit, which was added to have a sort of tone control. The parameter values of the unit are set as: $V_{\text{ref}} = 5.1$ V, $R_3 = R_4 = 10$ kΩ, $C_2 = 47$ nF, and $R_5 = 24$ kΩ.

Output Stage: In the original schematic, the output stage is composed of a common-emitter amplifier, which sums the phase-shifted and the original signals together, and by a high-pass filter with cut-off frequency $f_{\text{c}} = 22$ Hz. The latter is responsible for removing DC components from the output. In this manuscript, however, we consider the output stage shown in Fig. 3, where the original PNP Bipolar Junction Transistor (BJT) is omitted as its nonlinear effect is considered to be negligible; the amplification factor together with the inverting action originally brought in by the common-emitter amplifier are found sufficient to be modeled by means of a (negative) make-up gain in post-processing. In addition, in Fig. 3 V_1 is the output of the input buffer (dry signal),

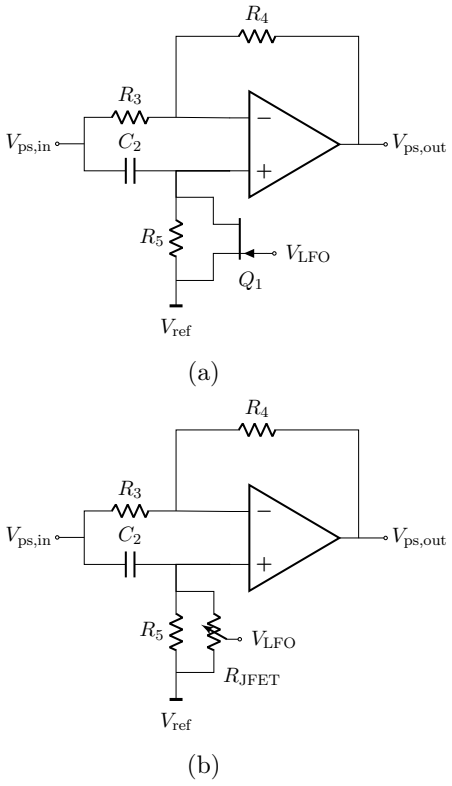

Figure 2: *(a) Schematic of the MXR Phase 90 shifting unit. (b) Phase-shifting stage where the JFET transistor is modeled via the proposed time-varying resistor approximation.*

whilst V_2 is the output of the cascade of phase-shifting units. When the processed signal is added to the original signal, a notch at w_{b} is created causing amplitude cancellation. The effect is enhanced if the notches are moved up and down in frequency and the easiest way to arrange this is by acting on R_{JFET}. This is achieved via the LFO that, by modulating the JFET gate voltages, acts on the drain-source resistance. The parameter values are the following: $C_3 = 47$ nF, $R_6 = 150$ kΩ, and $R_7 = 56$ kΩ.

4. JFET TIME-VARYING RESISTOR MODEL

In this section, we describe the proposed time-varying model of the n-JFET transistor in Fig. 2(a) that will be employed later on for the phaser simulation.

Contrary to BJTs, a JFET is a voltage-controlled device and does not require a biasing current [32]. Thus, the input impedance is, typically, in the order of 10^{10} Ω causing a very low gate current i_{g}. The electric charge flows between drain and source when a particular voltage is applied between gate and source. For instance, for an n-JFET to be on, it is required to impose a gate-source voltage $v_{\text{gs}} > 0$. As v_{gs} decreases, the drain-source current decreases as well, until the so-called *pinch-off*, where no conduction is present anymore. The voltage $v_{\text{gs}} = V_{\text{p}}$ for which such a condition is verified is called *pinch-off* voltage (a manufacturing constant, typically in the range $[-5, -1]$ V). When active, a JFET can operate in two distinct regimes [32]: (i) the *ohmic (or lin-*

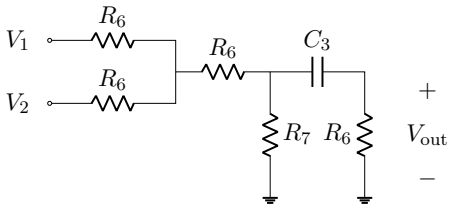

Figure 3: *Considered approximation of the schematic of the MXR Phase 90 output stage, where V_1 is the output of the input buffer stage, while V_2 is the output of the cascade of phase-shifting units.*

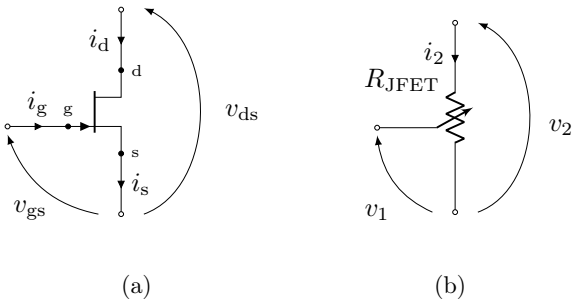

Figure 4: *(a) Circuit symbol of the JFET reporting the current and voltage conventions employed in this work. The drain terminal is marked with "d," the gate terminal with "g," while the source terminal with "s." (b) Proposed time-varying resistor approximation.*

ear) region, where the transistor operates as a voltage-controlled nonlinear resistor; (ii) the *saturation region*, where the transistor operates as a voltage-controlled current amplifier.

Let us now introduce the constitutive equations of an n-JFET transistor [32] according to the conventions reported in Fig. 4(a). Considering the on-region, the drain current i_d can be written as follows [33]

$$i_\text{d} = \begin{cases} \dfrac{2I_{\text{S0}}}{V_\text{p}^2}\left((v_\text{gs}-V_\text{p})-\dfrac{v_\text{ds}}{2}\right)v_\text{ds} & v_\text{gs}-V_\text{p} \geq v_\text{ds} \geq 0 \\ I_{\text{S0}}\left(1-\dfrac{v_\text{gs}}{V_\text{p}}\right)^2(1+\lambda v_\text{ds}) & v_\text{ds} \geq v_\text{gs}-V_\text{p} \geq 0 \end{cases}, \tag{11}$$

where λ is the parameter modeling the Early effect and I_{S0} is the saturation current at zero gate-source voltage [32]. Moreover, we can write the following equalities

$$\begin{aligned} i_\text{g} &= 0\,, \\ i_\text{s} &= i_\text{d}\,, \end{aligned} \tag{12}$$

where i_g and i_s are the gate and source currents, respectively. Note that the null gate current models the low current flowing into the gate itself due to the high gate impedance [32]. Finally, during off condition, i.e., $v_\text{gs} - V_\text{p} < 0$, the drain current is null, while (12) still holds true.

4.1. Kirchhoff Domain

We now present the proposed model of a time-varying resistor approximating the behavior of the n-JFETs in the MXR Phase 90

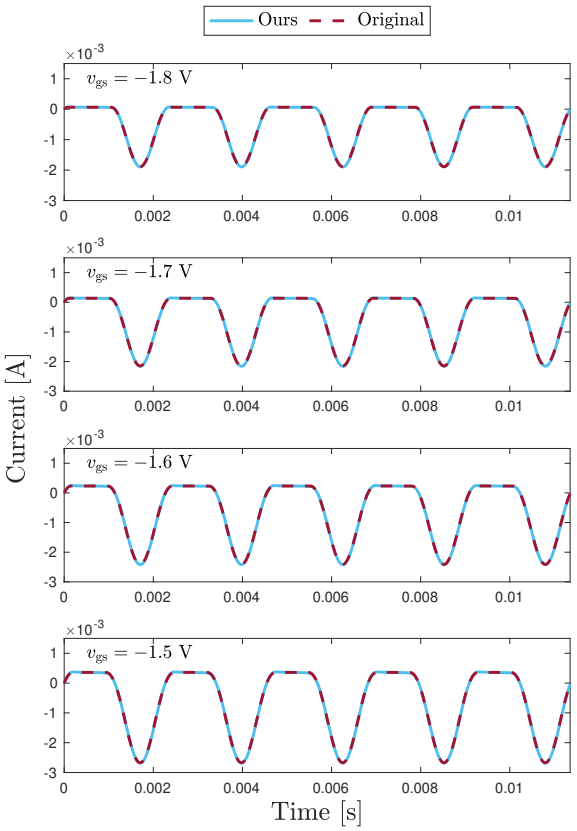

Figure 5: *Comparison between the JFET current computed with the traditional model ("Original", dashed red curve) and the current of the R_{JFET} element computed by means of the proposed WD model ("Ours", continuous blue curve), considering the approximation $v_2[k] \approx v_2[k-1]$.The overlap between each pair of curves confirms the accuracy of the representation.*

circuit. As already discussed in Section 3, the JFET is used to vary the resistance seen by the capacitor C_2 such that the phase-shift introduced by the all-pass filter can move in frequency. In light of this consideration, we can obtain the equivalent resistance in each of the JFET conducting regions by taking into account the resistor constitutive equation

$$R_\text{JEFT} = \frac{v_\text{ds}}{i_\text{d}}\,. \tag{13}$$

Hence, starting from (11) and (13) and considering the conventions reported in Fig. 4(b), we can write the equation of such a time-varying resistor directly in the discrete-time domain as follows

$$R_\text{JEFT}[k] = \begin{cases} R_\text{ohm}(v_1[k], v_2[k]) & v_1[k]-V_\text{p} \geq v_2[k] \geq 0 \\ R_\text{sat}(v_1[k], v_2[k]) & v_2[k] \geq v_1[k]-V_\text{p} \geq 0 \\ \infty & v_1[k]-V_\text{p} < 0 \end{cases} \tag{14}$$

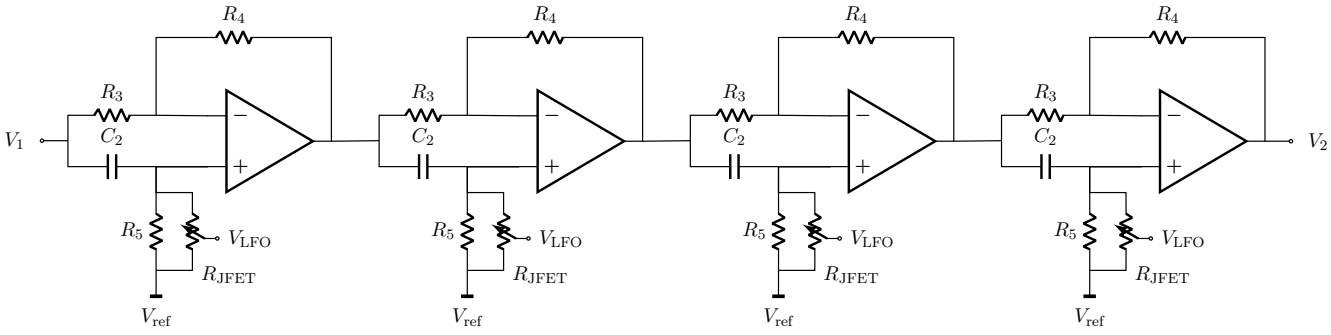

Figure 6: *Cascade of four phase-shifting units (see Fig. 2(b)) constituting an approximation to the overall MXR Phase 90 phase-shifting stage. V_1 is the output of the Input Buffer Stage shown in Fig. 1, whilst V_2 is the output of the cascade that will be mixed with V_1 in the Output Stage for obtaining the phasing effect.*

with

$$R_{\text{ohm}}\left(v_1[k], v_2[k]\right) = \frac{V_{\text{p}}^2}{2I_{\text{S0}}\left(v_1[k] - V_{\text{p}} - \dfrac{v_2[k]}{2}\right)}\,, \tag{15}$$

$$R_{\text{sat}}\left(v_1[k], v_2[k]\right) = \frac{v_2[k]}{I_{\text{S0}}\left(1 - \dfrac{v_1[k]}{V_{\text{p}}}\right)^2 \left(1 + \lambda v_2[k]\right)}\,, \tag{16}$$

where k is the sample index, v_1 is the voltage between ground and the control terminal, whilst v_2 is the voltage on the resistor itself. Finally, the R_{JFET} voltage v_2 is computed by means of the well-known Ohm's law according to the traditional circuit theory. In particular, it is worth to explicitly write down the parameters of the Thévenin equivalent model shown in (2),

$$R_{\text{e}}[k] = R_{\text{JFET}}[k]\,, \qquad V_{\text{e}}[k] = 0\,, \tag{17}$$

as these will be useful in the next section for deriving the relative WD equivalent.

4.2. Wave Digital Domain

Although being very compact, the model presented in the previous section is, unfortunately, implicit. This is due to the instantaneous dependence of (16) on voltage $v_2[k]$, which is known only after the working point at sample k is determined. Thus, in order to obtain an explicit model, we may approximate the current value of v_2 with its past value, i.e., $v_2[k] \approx v_2[k-1]$, with the assumption that, for a certain sampling frequency f_{s}, the past value is very close to the current one. Such an approximation should be considered even in the WD domain, given that by directly applying the definition of waves reported in (1) to (14), we obtain a WD model that cannot be adapted.

Starting from the Thévenin equivalent parameters reported in (17), equation (3) and the consideration thereof, as well as using the approximation $v_2[k] \approx v_2[k-1]$, we can write the wave b_2 reflected by the R_{JFET} element as follows

$$b_2[k] = V_{\text{e}}[k] = 0\,, \tag{18}$$

Table 1: *Parameters for modeling the 2N5952 JFET [34].*

Parameter	Value
V_{p}	-2.021 V
I_{S0}	5.367 mA
λ	4×10^{-3}

with

$$Z_2[k] = R_{\text{e}}[k] = \\ = \begin{cases} R_{\text{ohm}}(v_1[k], v_2[k-1]) & v_1[k] - V_{\text{p}} \geq v_2[k-1] \geq 0 \\ R_{\text{sat}}(v_1[k], v_2[k-1]) & v_2[k-1] \geq v_1[k] - V_{\text{p}} \geq 0\,, \\ \infty & v_1[k] - V_{\text{p}} < 0 \end{cases} \tag{19}$$

where Z_2 is its port resistance. The hypothesis $v_2[k] \approx v_2[k-1]$, in fact, allows us to obtain an explicit WD model that can be adapted as any resistor, according to what explained in Section 2.

In order to test the accuracy of the proposed WD model, we compare it to the original formulation of (11). As reference JFET, we consider the 2N5952 [34], i.e., the transistor employed in the MXR Phase 90, whose parameters are reported in Table 1. Moreover, we set $v_{\text{ds}} = v_2 = A\sin\left(2\pi k f_0 / f_{\text{s}}\right)$, with amplitude $A = 1$ V, fundamental frequency $f_0 = 440$ Hz, and sampling frequency $f_{\text{s}} = 96$ kHz. The results are shown in Fig. 5, where each subplot is obtained with a different value of v_{gs} taken from the set $\{-1.8, -1.7, -1.6, -1.5\}$ V. In particular, the continuous blue curves represent the current of the JFET obtained with our approach (named "Ours") in the WD domain, while the dashed red curves represent the results obtained with (11) (named "Original") in the Kirchhoff domain. The overlap between the different curves points out the accuracy of the proposed representation. With the aim of providing an objective metrics to evaluate the model, we compute the Mean Squared Error (MSE) between each pair of curves and then we average the results; this yields $\overline{\text{MSE}} = 1.23 \times 10^{-10}$. We then run the same test but with $f_0 = 10$ kHz obtaining $\overline{\text{MSE}} = 6.76 \times 10^{-8}$, which stresses even further the accurate performance of our approach.

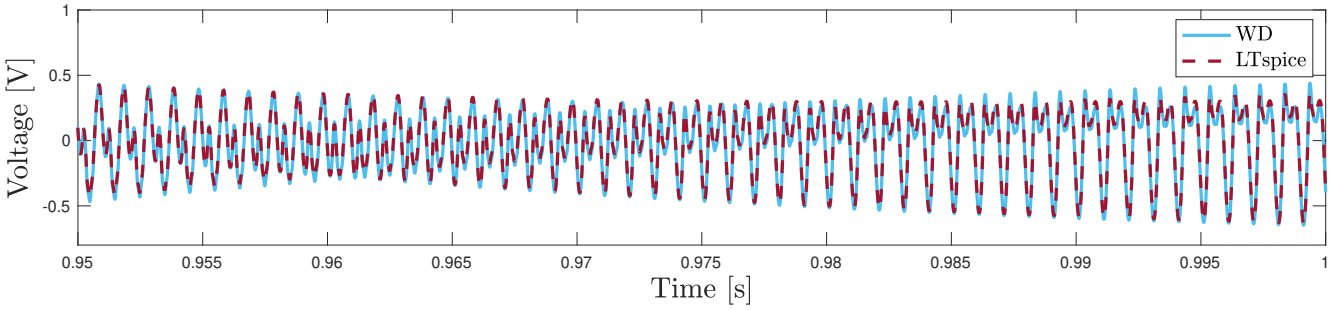

Figure 7: *Output voltage V_{out}. The continuous blue curve represents the WD implementation, while the dashed red curve the LTspice implementation.*

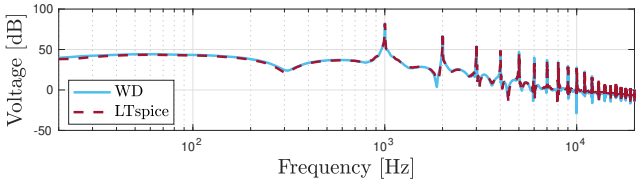

Figure 8: *Discrete Fourier Transform (DFT) of the simulation results.*

Finally, the proposed R_{JFET} element is employed in lieu of the JFET element of the phase-shifting unit shown in Fig. 2(a), leading to the stage represented in Fig. 2(b).

5. WD MXR PHASE 90 EMULATION

In this section, we provide the description of the overall WD emulation of the MXR Phase 90. The reference circuit that we consider is composed as follows: the input signal is fed to the input buffer stage shown in Fig. 1, whose output V_1 serves as inputs to the phase-shifting stage shown in Fig. 6. This in turn consists of four phase-shifting units like the one shown in Fig. 2(b), where each single unit sees its JFET substituted with the proposed R_{JFET} component. Then, V_1 and V_2 are used as input to the output stage represented in Fig. 3, which will finally provide the output of the processing chain. In our WD implementation, each of the aforementioned stages, as well as each phase-shifting unit, is modeled as standalone circuits and then combined together following the very same chain described above. To this aim, additional load resistances (e.g., 1 GΩ) are added to the subcircuits with the purpose of reading the output voltage that is then fed to the next stage.

Each circuit is implemented in the WD domain using a single topological junction (the root of the WDF tree) to which all the elements are connected, following an approach similar to what shown in [27]. Given that resistive sources can be adapted [4], voltage sources (e.g., V_{ref}, V_{in}, etc.) are implemented as resistive sources by exploiting the resistances that are in series; if no series resistance is present, a small series resistance is added to the source model (e.g., 1 μΩ). Moreover, for the circuits containing opamps, the approach proposed in [10] is used to encompass them into scattering matrices. In fact, we consider such opamps to be ideal and thus to be fully described by *nullors*, which can be then treated as connection elements following the double digraph method shown in [10]. In particular, the scattering matrix for the circuit shown in Fig. 1 can be computed substituting into (6)

$$\mathbf{Q}_{\text{V}} = \begin{bmatrix} 1 & 0 & -1 & -1 \\ 0 & 1 & -1 & -1 \end{bmatrix}, \quad \mathbf{Q}_{\text{I}} = \begin{bmatrix} 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 \end{bmatrix}, \tag{20}$$

for the circuit shown in Fig. 2(b) substituting into the same equation

$$\mathbf{Q}_{\text{V}} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & -1 & -1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & -1 & -1 \end{bmatrix},$$
$$\mathbf{Q}_{\text{I}} = \begin{bmatrix} 1 & 0 & 0 & 0 & -1 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \end{bmatrix}, \tag{21}$$

whereas for the circuit shown in Fig. 3 substituting into (4)

$$\mathbf{Q} = \begin{bmatrix} 1 & 0 & 0 & -1 & 1 & -1 \\ 0 & 1 & 0 & -1 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 & -1 \end{bmatrix}. \tag{22}$$

As far as the circuit shown in Fig. 1 is concerned, ports ranging from 1 to 4 are connected to V_{in} (with series resistance R_1), R_{L} (load resistance), C_1, and V_{ref} (with series resistance R_2). As for the circuit shown in Fig. 2(b), ports ranging from 1 to 8 are connected to $V_{\text{ps,in}}$ (with a small series resistance), R_5, R_3, C_2, R_4, R_{JFET}, R_L (load resistance), V_{ref} (with a small series resistance), while, regarding the circuit shown in Fig. 3, ports ranging from 1 to 6 are connected to V_2 (with series resistance R_6), R_6, C_3, R_7, V_1 (with series resistance R_6), and R_6 (output). Every element is then adapted according to the considerations reported in Section 2, and the trapezoidal rule is employed for the approximation of the time derivatives characterizing the constitutive equation of capacitors.

In order to test the accuracy of the overall WD implementation, we realize the original circuit (considering all the transistors) in LTspice, which is a well-known circuit simulation software. The JFET elements are modeled taking into account the parameters reported in Table 1. Then, we set $V_{\text{in}} = A \sin(2\pi k f_0 / f_s)$, with $A = 1$ V, $f_0 = 1$ kHz, and $f_s = 96$ kHz. Moreover, we set the LFO equal to a triangular wave with an offset of 3.25 V, an amplitude of 0.15 V, a fundamental frequency of 2 Hz, and a duty cycle

Figure 9: *MXR Phase 90 plug-in on Logic Pro X.*

of 65%; the duration of the input as well as the LFO is set to be 1 s. Fig. 7 shows the output voltage of the processing chain, in particular the last 50 ms. The red dashed curve representing the LTspice implementation is overlapped with the continuous blue curve representing the WD implementation, pointing out the good accuracy of the representation. Looking at Fig. 7, we can state that the two curves share the same phase, but, although negligible, some errors are present on the peak amplitudes. With the purpose of providing an objective assessment of the model accuracy, we compute the MSE between the two curves all over the simulation time and we obtain $\mathrm{MSE} = 4.1 \times 10^{-4}$, which confirms the good performance of the approach. Finally, Fig. 8 shows the Discrete Fourier Transform (DFT) of the simulation results. The dashed red curve is once again overlapped to the continuous blue curve, proving the model to be accurate even in the frequency domain, with a Mean Absolute Value (MAE) of 1.62 dB.

The WDF, realized by means of a plain MATLAB script, together with LTspice files, is available at: `github.com/polimi-ispl/mxrphase90`. Audio examples are, instead, available on the following GitHub page: `polimi-ispl.github.io/-mxrphase90`. Such audio samples reveal that, from a perceptual standpoint, the output of the original circuit (marked with "LTspice") and the output of our WDF (marked with "Ours") are practically indistinguishable.

Finally, we provide a real-time plug-in realized within the JUCE framework [26], a possible use of which is shown in Fig. 9; this is available for free on our repository. The plug-in is characterized by a low CPU usage (around 0.5% at 44.1 kHz on an Apple M1 Pro) and can be thus readily used by passionate musicians in search for the sound of yesteryear.

6. CONCLUSIONS

In this paper, we addressed the emulation of the MXR Phase 90, a famous phaser of the late '70s which still owns a foothold into guitar players' pedalboard. In particular, we proposed an efficient and explicit WD realization that maintains a good level of accuracy. In order to achieve such a goal, we introduced an explicit model for the JFET elements characterizing the effect phase-shifting units. Starting from the evidence that JFETs, in this scenario, are employed just to vary the equivalent resistance seen by the all-pass filter capacitors, we proposed to substitute the transistor with a variable resistor that takes the value of the JFET channel resistance. To test the accuracy of the representation, we compared the output of our WD implementation with the output of an LTspice simulation, obtaining a low MSE. Finally, besides providing audio examples for the interested readers, we build and freely provide a real-time plug-in using the JUCE framework in order to demonstrate the applicability of the proposed physical model.

Future work may entail the emulation of other modulation effects, such as chorus pedals or flangers, in order to further test the advantages given by WDFs in solving circuits with time-varying phenomena.

7. ACKNOWLEDGMENTS

The authors would like to thank the anonymous reviewers for their valuable comments and suggestions.

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