DIGITIZING THE SCHUMANN ELECTRONICS PLL ANALOG HARMONIZER

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ABSTRACT

The Schumann Electronics PLL is a guitar effect that uses hardware-based processing of one-bit digital signals, with op-amp saturation and CMOS control systems used to generate multiple square waves derived from the frequency of the input signal. The effect may be simulated in the digital domain by cascading stages of state-space virtual analog modeling and algorithmic approximations of CMOS integrated circuits. Phase-locked loops, decade counters, and Schmitt trigger inverters are modeled using logic algorithms, allowing for the comparable digital implementation of the Schumann PLL. Simulation results are presented.

1. INTRODUCTION

The Schumann PLL [1], standing for phase-locked loop—the integrated circuit that the effect is designed around—is a fuzz and harmony processor that uses primitive digital processing techniques to create distorted chords. It is functional with most instrument inputs, but was primarily designed with the guitar in mind [2]. The effect derives three distinct square waves from an input signal, one at the fundamental frequency of the input, and at two new frequencies relative to the fundamental of the input. Since the pedal is designed to lock on to one frequency it is primarily intended to accept monophonic signals.

The Schumann PLL features many user-accessible parameters in its interface, providing a large range of control over the effect, yet contributing to performance issues at some settings, such as no output or self-oscillation. The tonal character of the unit is that of a glitchy-sounding fuzz harmonizer that can be tuned to ramp up into a locked tone or waver in and out of a pitch to which it is frequency-locked.

The signal path of the effect includes pre-amplification followed by square wave saturation. The saturated signal is then fed into a digital logic circuit that generates a phase-aligned, frequency multiplied copy of the signal. The frequency-multiplied signal is then further divided to achieve a sub-harmonic. The three output square waves result in a harsh, harmonically rich tone. This signal path is outlined in detail in fig. 1.

Previous work has addressed phase-locked loops (PLLs) in audio software for monophonic pitch tracking, demonstrating their ability to lock onto a single frequency and detect pitch [3]. Existing software implementations of PLLs typically focus on high-level signal processing blocks [4][5]. This work addresses this gap

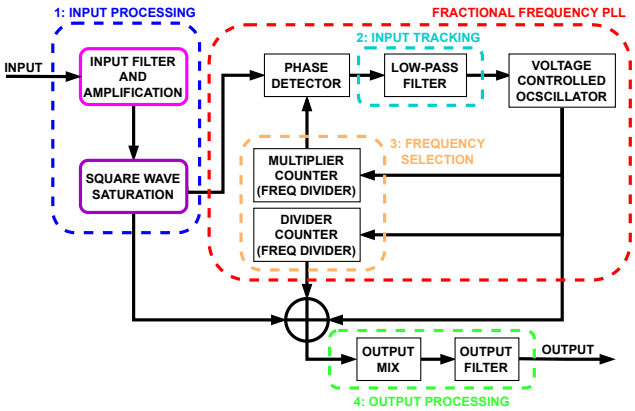

Figure 1: *Signal path block diagram, numbered outlines represent user controllable stages.*

Figure 2: *Schumann PLL interface [1].*

by incorporating component-level modeling of filter and preamplification stages, ensuring accurate emulation of analog stages, some of which significantly influence the behavior of digital components (see section 4.2.2). Further, included analyses of logic systems are grounded in the datasheets of the integrated circuits used in the original pedal design, providing a comprehensive model for digital emulation of the Schumann PLL. This novel approach ensures accurate emulation of both the analog circuitry and the digital logic, providing a perceptually and analytically similar software replication of the original hardware.

In Section 2, we outline the general user controlled parameters and output variation achievable with the effect. In Section 3 we present state-space solutions for the modeling of the analog input circuit. Section 4 outlines the approaches developed for

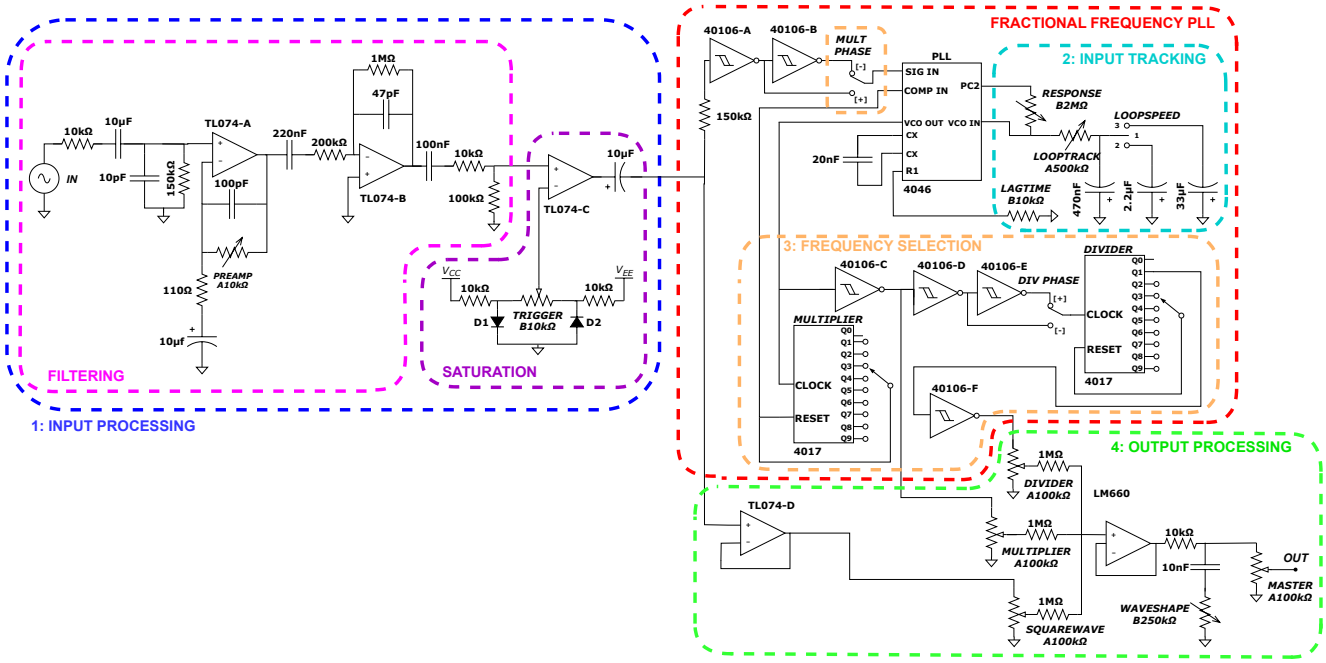

Figure 3: *Full circuit diagram of the Schumann PLL [6].*

the real-time modeling of CMOS digital integrated circuits. Finally, these functions are compiled into a functioning MATLAB [7] script and analyzed in comparison to a hardware replica of the Schumann PLL in Section 6, and conclusions are presented in 7. The MATLAB script and sound examples may be accessed at the accompanying GitHub repository [1].

2. OPERATION OF THE PLL

The interface of the Schumann PLL, shown in fig. 2, is significantly more complex than that of a standard effect pedal, with fifteen user accessible parameters. The controls may be separated into four groups that correspond to function blocks in fig. 1, represented by the dashed boxes 1-4. These sections highlight the functional groupings of the control interface and are not wholly representative of the internal behavior of the effect—it is necessary to note that there may be interaction between the setting choices in these groups due to the feedback loop of the PLL. These control interface groups are mapped to their respective sub-circuits in fig. 3.

The **pre amp** and **trigger** knobs control how the instrument signal is preprocessed before the digital logic processing. **Pre amp** controls input amplification and filtering and **trigger** controls the duty cycle of the input-derived square wave.

The **loop track** and **response** knobs, and the **loop speed** toggle set component values in an analog RC filter responsible for smoothing control voltage passed to the voltage-controlled oscillator (VCO) that generates the upper harmonic. These controls interact with the **lag time** parameter, which adjusts the internal gain of the VCO.

The **multiplier** and **divider** rotary controls set the frequency of the harmonic and sub-harmonic generated tones. The **multiplier phase** and **divider phase** controls simply invert the phase of the multiplied and divided synthesized signals.

The **square wave**, **multiplier**, and **divider** knobs adjust the gain relationship between the three generated square waves. **Wave shape** controls an output low-pass filter, and **master** determines the master output level of the pedal.

[1] https://github.com/ijfarrell/dafx24

3. ANALOG INPUT PROCESSING

The analog input circuit corresponds with the first stage of the signal path (fig. 1), consisting of the input filtering and square wave generation functions. The circuit schematic appears in fig. 3 and shows the electronic components of the analog input circuit, outlined in blue. This circuit can be separated into two stages. The first stage is outlined in pink, filtering and amplifying the input signal. The second stage, outlined in purple, uses an op-amp comparator to saturate the filtered signal prior to digital processing.

3.1. Input Filter

The first stage of analog pre-processing is the analog input filter. This filter can be divided into two sub-stages, outlined in red and blue in fig. 4. The primary function of the stages is to filter out the low and high frequencies of the input signal to preserve the fundamental frequency of the input signal in the generated square wave. This filtering improves the tracking in the frequency-locked synthesized signals. The secondary purpose of these stages is to significantly amplify the input signal. In the case of a guitar input, one of the primary intended use cases, it boosts the dymamic signal of guitar pickups in the 100 mV to 1 V peak to peak range to the 10 V range.

To model the analog filtering, linear state-space modeling will be employed, which can be used to represent the behavior of an analog circuit in continuous time [8]. The following equations

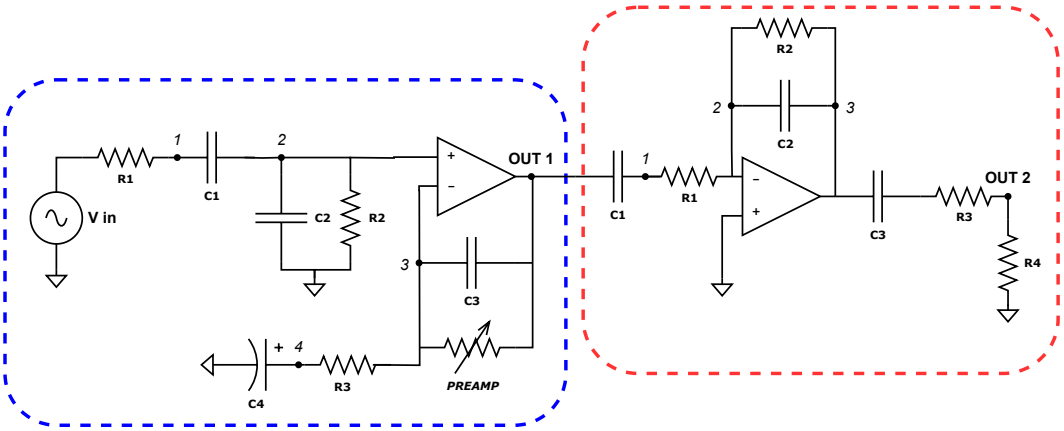

Figure 4: *Two-stage analog input filtering and amplification, separated into two stages for cascaded state-space representation [6].*

are a conventional configuration to represent the state of a linear time-invariant system in the single-input/single-output case, which captures the characteristics necessary for the analog portion of the Schumann PLL:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{b}u(t), \tag{1a}$$

$$y(t) = \mathbf{c}^T\mathbf{x}(t) + du(t), \tag{1b}$$

where u is the input, $\mathbf{A}$ is the $N \times N$ state matrix, $\mathbf{x}$ is the $N \times 1$ state vector, with $\dot{\mathbf{x}}$ as its derivative, $\mathbf{b}$ and $\mathbf{c}$ are $N \times 1$ vectors, d is the feedthrough constant, and y is the output. The state-space is implemented using trapezoidal integration, which approximates $\dot{\mathbf{x}}(t)$ as a straight line between $n-1$ and n [9].

Through nodal analysis [10], the labeled nodes and components presented in fig. 4 may be used to obtain the system of differential equations of the red and blue outlined sub-circuits. Corresponding component values are shown in fig. 3. The following state-space is of the capacitor voltages $\dot{v}_{C_1}$, $\dot{v}_{C_2}$, $\dot{v}_{C_3}$, and $\dot{v}_{C_4}$, in the blue-outlined section in fig. 4, with the input at V_{in} and output at OUT 1:

$$\mathbf{A} = -\begin{bmatrix} 0 & -1 & 0 & 0 \\ \frac{1}{C_1C_2R_1R_2} & \frac{C_1(R1+R2)+C_2R_2}{C_1C_2R_1R_2} & 0 & 0 \\ 0 & -\frac{R_1C_1}{C_4R_3} & \frac{1}{R_{preamp}C_3} & \frac{1}{R_3C_3} \\ 0 & -\frac{R_1C_1}{C_4R_3} & 0 & \frac{1}{R_3C_4} \end{bmatrix}, \tag{2a}$$

$$\mathbf{b} = \begin{bmatrix} 0 \\ \frac{1}{C_1C_2R_1R_2} \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{c} = \begin{bmatrix} 0 \\ R_1C_1 \\ 1 \\ 0 \end{bmatrix}, \quad d = 0. \tag{2b}$$

The second stage of the analog input preamp is outlined in red in fig. 4. This stage consists of an op-amp integrator amplifier and an output high-pass filter voltage divider configuration. The amplification in this stage is significantly higher than the first as well as the attenuation outside of the pass band, resulting in a substantially band passed output. The input capacitor C_1 attenuates the low frequency content of the signal from the prior stage. To calculate the state space solution of this stage, the same method used in the first stage will be applied. The following represents the system derived from the circuit outlined in red in fig. 4, with the input at OUT 1 and output at OUT 2. The following state is of the capacitor voltages are $\dot{v}_{C_1}$, $\dot{v}_{C_2}$, and $\dot{v}_{C_3}$, in the red-outlined section in fig. 4:

$$\mathbf{A} = \begin{bmatrix} -\frac{1}{R_1C_1} & 0 & 0 \\ \frac{1}{R_1C_2} & -\frac{1}{R_2C_2} & 0 \\ \frac{1}{R_1C_3} & -\frac{1}{R_2C_3} & -\frac{1}{(R_3+R_4)C_3} \end{bmatrix}, \tag{3a}$$

$$\mathbf{b} = \begin{bmatrix} \frac{1}{R_1C_1} \\ -\frac{1}{R_1C_2} \\ -\frac{1}{R_1C_3} \end{bmatrix}, \quad \mathbf{c} = \begin{bmatrix} 0 \\ \frac{R_4}{R_3+R_4} \\ \frac{R_4}{R_3+R_4} \end{bmatrix}, \quad d = 0. \tag{3b}$$

With the state space matrices represented above, the filters may be implemented using trapezoid rule [9]. The transfer function of the preamp filters are shown in fig. 5.

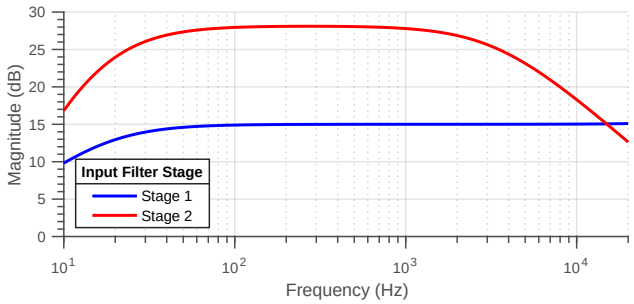

Figure 5: Output from cascaded input filter stages. **Pre amp** = 5.

3.2. Analog Saturation

The circuit employs two stages of saturation in series. The first stage is an op-amp comparator with a variable DC offset control. Fig. 6 shows the topology in the circuit and a simplified model. V_{CC} and V_{EE} are the 11.85 V and −11.85 V rails of the circuit, respectively, and $R_1 = R_2 = R_{\text{Trigger}}$, where R_{Trigger} is the resistance of the **trigger** potentiometer. The diodes in this configuration are 1N4001 rectifier diodes [11], with a current of 1 mA thorugh the diodes in the effect, the forward voltage is .60 V. This allows for a range of −.60 V to .60 V on the inverting op-amp input, controlled by the **trigger** potentiometer.

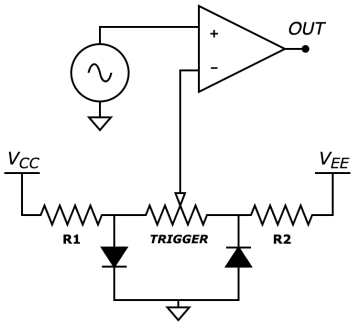

Figure 6: *Op-amp comparator stage with offset control [6].*

With the **trigger** knob position variable from 0 to 1, $0 \leq \eta \leq 1$, the open loop gain of the op-amp $V_o l$ may be represented with the following equation:

$$V_{ol} = A_o(V_+ - .60(2\eta - 1)), \tag{4}$$

where A_o is the open loop gain and V_+ is the input to the non-inverting terminal of the op-amp. Accounting for the supply voltage and variable trigger voltage, the following represents the output of the Schumann PLL op-amp comparator stage with open loop output voltage V_{ol}:

$$V_{\text{out}} = \begin{cases} V_{CC}, & V_{ol} > V_{CC}, \\ V_{ol}, & V_{EE} \leq V_{ol} \leq V_{CC}, \\ V_{EE}, & V_{ol} < V_{EE}. \end{cases} \tag{5}$$

The function of this variable **trigger** comparator circuit is to reject input noise from inclusion in the 1-bit processing of the following effect stages, since only voltage differential across the set DC voltage comprises the output waveform.

4. DIGITAL PROCESSING

The Schumann PLL is partly an analog audio effect; however, the circuit primarily relies on mixed signal integrated circuits (ICs) [6] that integrate digital logic and analog functionality. While the pedal does not use conventional digital signal processing techniques (e.g. it does not utilize a sophisticated ADC, DAC, or microprocessor), it uses hardware-implemented digital logic blocks for simple operations on one-bit signals, such as phase comparison and counting [12, 13]. These simple digital logic processes are implemented via CMOS integrated circuits, and specifically 4000 series ICs developed in the 1970s [14].

Complementary metal-oxide-semiconductor (CMOS) is a technology that uses p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to implement digital logic in integrated circuit designs [10]. This approach allows for low level digital circuits with a high degree of responsiveness. These ICs have a low transition time, usually on the order of tens to hundreds of nanoseconds. When using these ICs in the processing of analog audio signals, this suggests that there is not a need for component-level analog modeling of CMOS, since they transition at a substantially higher rates than typically would be captured in audio rate sampling [15], but rather capturing the breadth of their functionality through a digital logic implementation. As such, in this digitization effort these circuits are simply implemented with conditional logic in accordance with their data sheets, with limited consideration for component-level modeling. The schematic for the digital circuit is shown in fig. 3, outlined in red.

There are three distinct CMOS integrated circuits present in the effect. The first is the 40106 Schmitt trigger inverter [15], which further converts the incoming op-amp comparator signal into a true one-bit digital signal (while also inverting it). The second is the 4046 phase-locked loop (PLL) [12], a multi-stage synthesizer designed to match the frequency of its output to that of an input signal. The third and final is the 4017 decade counter [13], which is used for frequency division.

4.1. Inverters

The Schmitt trigger inverter is a one-bit analog to digital converter. It behaves as a threshold voltage detector. The circuit behaves similarly to a comparator, outputting a fixed voltage when the input signal exceeded a certain threshold, yet has hysteretic behavior. [10]. It uses positive feedback in a circuit to set two threshold voltages, the current state and recent past state, and triggers a low output when the voltage crosses the upper voltage threshold V_P while increasing, and a high output when the voltage crosses the lower threshold voltage V_N while decreasing. With the supply voltage in the Schumann PLL fixed at 11.85 V ($V_{\text{supply}} = 11.85$), the resulting threshold voltages in the Schmitt trigger are $V_P = 6.5$ V and $V_N = 4.5$ V [15].

The digital implementation of a Schmitt trigger is a system with one step of memory to mimic the feedback behavior of the trigger. This enables the system to access the current state of the system to determine the updated state.

Algorithm 1 40106 Schmitt trigger Digitization

$Input =$ Input signal
$\text{STATE} =$ Output state at current sample
$\text{STATE}_{\text{prev}} =$ Output state at previous sample
for n = 1:end **do**
  if $Input(n) \geq V_{\text{P}}$ and $Input(n-1) < V_P$ **then**
    $\text{STATE} = 0$
  end if
  if $Input(n) \leq V_{\text{N}}$ and $Input(n-1) > V_N$ **then**
    $\text{STATE} = V_{\text{supply}}$
  end if
  $\text{STATE}_{\text{prev}} = \text{STATE}$
end for

The algorithm 1 represents the digital implementation of the Schmitt-Trigger inverter. The transition time of the trigger is typically 45 ns for the 40106 IC [15], and can be safely ignored in an audio rate model.

4.2. Phase-locked Loop

The PLL IC used in the design of the Schumann PLL is the CD4046B CMOS micropower phase-locked loop, introduced by RCA in the 1970s—commonly used for clock multiplication in digital electronics [12]. The IC consists of a low-power linear voltage controlled oscillator and two types of phase comparators. In addition to the on-board functions, the PLL circuit requires two primary functions. The first of these functions is the loop filter, which smooths the output of the phase comparator, making it suitable for VCO input. The second is a method of frequency dividing the VCO output signal—this is done using the decade counter in the circuit. These functional blocks are presented in fig. 7

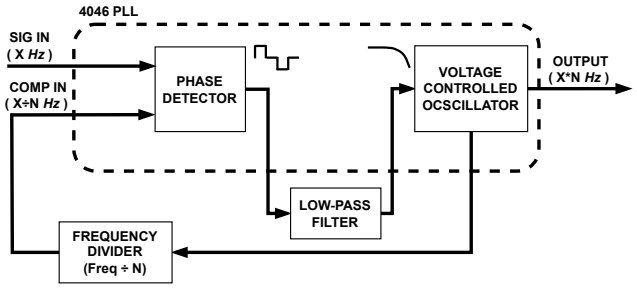

Figure 7: *Phase-locked loop system block diagram [16].*

4.2.1. Phase Frequency Detector

The input stage of the phase-locked loop is the phase detector, of which 4046 IC contains two differing methods. The type II phase comparator is used in the Schumann PLL design. The Phase Comparator II circuit is an edge controlled digital memory network [12] also known as a phase frequency detector (PFD) [16]. This method of phase detection uses a logic circuit (shown in fig. 8), acting only on the rising edges of the two signal inputs.

The system detects signal level discrepancies in the rising edges of the inputs SIG IN and COMP IN (feedback from the VCO out), outputting a high voltage when the COMP IN signal lags behind the SIG IN signal and a low voltage when the SIG IN signal lags behind the COMP IN signal.

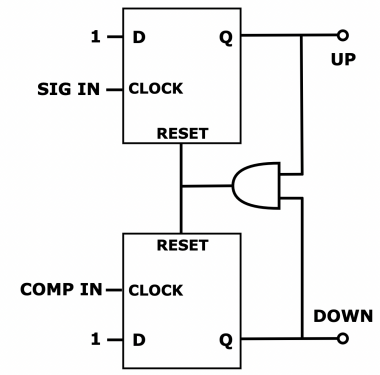

Figure 8: *Phase frequency detector logic diagram [16].*

Algorithm 2 is the digital implementation for square wave edge detection and output the signal of the PFD, where Q_{up} and Q_{down} are the upper and lower D Flip-Flop outputs, respectively, and HI_Z is the output flag for the the high impedance state for reference in the loop filter algorithm. V_{supply} represents the supply voltage output of the configuration, 11.85 V.

4.2.2. Loop Filter

The loop filter provides low-pass filtering, or smoothing, of the square wave output of the PFD, converting it to a variable DC control voltage for the VCO. The filter topology suggested by the 4046 data sheet [12] is a basic RC low-pass, and yet the Schumann PLL uses an RC configuration with a voltage divider and feedthrough pictured in fig.9, with the input signal from the phase detector passing through the filter and into the VCO control input.

Algorithm 2 4046 PC II (Phase Frequency Detector)

$\mathrm{N} =$ Number of samples in signal
$COMP_{\mathrm{in}} =$ COMP IN Input signal
$SIG_{\mathrm{in}} =$ SIG IN Input signal
$V_{\mathrm{contol}} =$ Control Voltage output
$Q_{\mathrm{up}} = 0$
$Q_{\mathrm{down}} = 0$
$HI_Z = 0$
for n = 1:N do
  if $SIG_{\mathrm{in}}(n) > 0$ and $SIG_{\mathrm{in}}(n-1) = 0$ **then**
    $Q_{\mathrm{up}} = 1$
  end if
  if $COMP_{\mathrm{in}}(n) > 0$ and $COMP_{\mathrm{in}}(n-1) = 0$ **then**
    $Q_{\mathrm{down}} = 1$
  end if
  if $Q_{\mathrm{up}} = 1$ and $Q_{\mathrm{down}} = 1$ **then**
    $Q_{\mathrm{up}} = 0$
    $Q_{\mathrm{down}} = 0$
  end if
  if $Q_{\mathrm{up}} = 1$ **then**
    $V_{\mathrm{contol}}(n) = V_{\mathrm{supply}}$
  end if
  if $Q_{\mathrm{down}} = 1$ **then**
    $V_{\mathrm{contol}}(n) = 0$
  end if
  if $Q_{\mathrm{up}} = 0$ and $Q_{\mathrm{down}} = 0$ **then**
    $HI_Z = 1$
  end if
end for

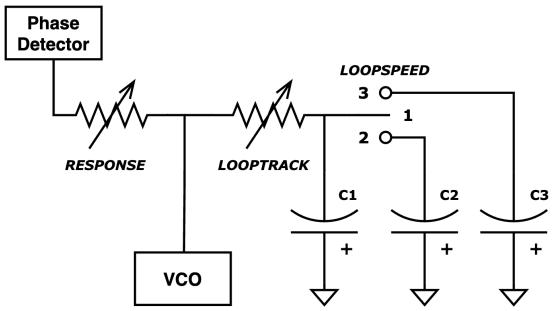

Figure 9: *PLL external loop filter schematic [6].*

The components of the filter consist of two user defined variable voltages, **response** and **loop track** and a switchable capacitance with **loop speed**. This allows the user to control the amount of unfiltered signal fed through, the tracking speed and variance of the VCO, and the frequency ramp and decay time, corresponding to the discharge time of the capacitor in the filter (seen in fig. 9), respectively.

In the configuration seen in the effect there may be two capacitors in parallel to ground, this may be represented as a single capacitance with the sum of any connected capacitors [10]. The following state equations are used to model the system:

$$\mathbf{A} = \frac{-1}{(R_{\text{response}} + R_{\text{looptrack}})C_{\text{loopspeed}}}, \quad (6a)$$

$$\mathbf{b} = \frac{1}{(R_{\text{response}} + R_{\text{looptrack}})C_{\text{loopspeed}}}, \quad (6b)$$

$$\mathbf{c} = 1 - \frac{R_{\text{looptrack}}}{R_{\text{response}} + R_{\text{looptrack}}}, \quad (6c)$$

$$d = \frac{R_{\text{looptrack}}}{R_{\text{response}} + R_{\text{looptrack}}}. \quad (6d)$$

The above equations are relevant for the simulation considering an input signal from the PFD. Under the condition where the charge pump is closed there is a high impedance, equivalent to a break in the circuit, at the phase detector signal input. With this condition, the only output to the VCO is the discharged voltage from the capacitors. For this case there is a secondary output filter matrix that excludes the input, state, and feedthrough matrices, as follows:

$$\mathbf{A} = \frac{-1}{R_{\text{looptrack}}C_{\text{loopspeed}}}, \quad (7a)$$

$$\mathbf{c} = 1, \quad (7b)$$

which may be implemented with a filter switching condition using the HI_Z state from algorithm 2. Fig. 10 demonstrates the effect of the switching **loop speed** capacitors on the frequency response.

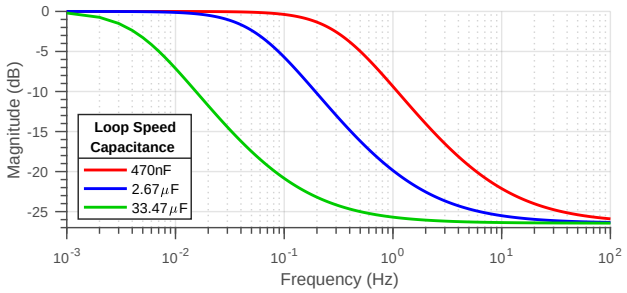

Figure 10: *PLL loop filter plot at all **loop speed** settings. **Loop track** = 50kΩ, **response** = 1MΩ.*

4.2.3. Voltage-Controlled Oscillator

The VCO uses the filtered control voltage from the phase comparator to generate a square wave at a designated frequency. The 4046 VCO is linear and designed to require low input voltages. As seen in the schematic fig. 3, the PLL requires an external capacitor and resistor to function. These components designate the VCO behavior, with the variable LAGTIME resistance controlling the center frequency of the frequency tracking and the external capacitor controlling bandwidth. These component values can be used to obtain a voltage to frequency coefficient with the following equation [16]:

$$f_{osc} = \frac{6.2(VCO_{\text{in}}/R_1)}{2C_1\frac{V_{CC}}{10} + 0.6}. \quad (8)$$

With this coefficient, the system can be approximated through the generation of a variable frequency sinusoid. This sinusoid may then be used to generate a square wave of the same frequency with the following:

$$\phi[n] = \left(\phi[n-1] + 2\pi\left(\frac{f_{\text{osc}}}{f_s}\right)\right) \mod 2\pi, \quad (9a)$$

$$\text{VCO}_{\text{out}}[n] = \text{sgn}(\sin(\phi[n])). \quad (9b)$$

This approach outputs a one-bit digital clock that accounts for the external PLL component values without necessitating the component-level modelling of the VCO.

4.3. Decade Counters

The decade counter performs the clock frequency division used for the sub-frequency and PLL feedback frequency generation. The IC used in the effect is the CD4017 CMOS counter, a 5-stage Johnson counter with 10 decoded outputs [13]. The logic circuit detects incoming rising clock edges, iterating through ten outputs. The timing of the output is dependent on the rotary position and configuration of the counters. The configuration of the counters with the rotaries are denoted in fig. 3, labeled **multiplier** and **divider**. The two decade counters in the circuit have slightly differing configurations.

Algorithm 3 4017 Multiplier Counter Implementation

```
N = Number of samples in signal
V_in = VCO generated input
RotarySetting = Rotary selection on counter chip
OutputDuration = Duration of output pulse in samples
OutputTimer = 0
InputPulseCount = 0
OutputState = 0
for n = 1:N do
  if V_in(n) > V_in(n − 1) then
    InputPulseCount = InputPulseCount + 1
    if InputPulseCount = RotarySetting then
      OutputState = 1
      InputCount = 0
      PulseTrigger = 1
    end if
  end if
  if OutputState = 1 then
    OutputTimer = OutputTimer + 1
    if OutputTimer = OutputDuration then
      OutputTimer = 0
      OutputState = 0
      InputPulseCount = 0
    end if
  end if
end for
```

The **multiplier** counter is found in the feedback path of the PLL, and routes the reset pulse to the COMP IN of the PLL PFD, resulting in a consistent output pulse width unrelated to the input frequency. The reset is theoretically instantaneous at the high output due to the direct feedback of output to reset pin. Physically the output pulse from the counter is determined by the propagation delay time of the 4017, at the supply voltage in the PLL this is $\sim$ 100 ns [13]. Modeling this exactly is not necessary in the PLL—instead a pulse width of 2 samples may be used to trigger the PFD model defined in section 4.2.1 and accurately reflect the maximum frequency of the sampling rate. The **divider** decade counter is configured to send output on the first detected clock edge

after reset, and is reset by a subsequent input clock. The primary functional difference is the lack of a unison frequency selection for the **divider** configuration, reflected in the pedal interface (fig. 2). Algorithms 3 and 4 outline the framework and differences in implementation between the two counter configurations.

Algorithm 4 4017 Divider Counter Implementation

```
N = Number of samples in signal
V_in = VCO generated input
RotarySetting = Rotary selection on counter chip
InputPulseCount = 0
OutputState = 0
for n = 1:N do
  if V_in(n) > V_in(n − 1) then
    InputPulseCount = InputPulseCount + 1
    if OutputState = 1 then
      OutputState = 0
    end if
    if InputPulseCount = RotarySetting then
      InputPulseCount = 0
      OutputState = 1
    end if
  end if
end for
```

5. ANALOG OUTPUT PROCESSING

The output of the effect after the digital processing consists of a summing amplifier configuration and a low-pass filter controlled by the **wave shape** knob on the effect interface. Each square wave signal has a volume control before the summing amplifier, allowing the user to scale the relative output amplitudes. The op-amp pictured is a single source voltage supplied to a LM660CN [17] CMOS op-amp with a single supply voltage, and will have a negative voltage limit of 0 V. To achieve this in the digital implementation, the signals may be added and then the output limited using a conditional statement.

The output low-pass filter is functionally identical to the loop filter topology, with the exception of the switchable capacitors. Fig. 11 documents the variable cutoff and high frequency attenuation from the variable filter resistance.

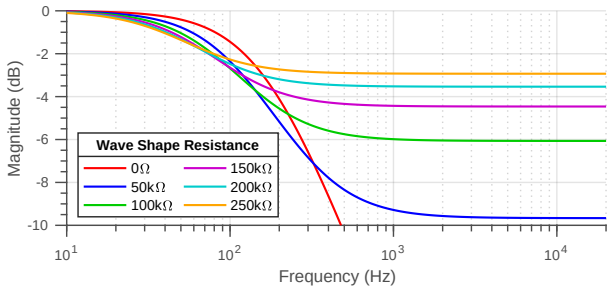

Figure 11: *Plot of output filter transfer function at variable* ***wave shape*** *resistances.* $R = 10\text{k}\Omega$, $C = 10\text{nF}$.

6. RESULTS

To document the performance of the digital model, it has been measured against a hardware clone of the Schumann built by the first author for the purpose of testing and analysis. This method of analysis is important, given the relative complexity of the system.

The square wave saturation on the signal input is generated through the op-amp clipping stage outlined in section 3. When isolated, the resultant output with a 200 Hz sine wave input is shown compared to the hardware output in the time domains in fig. 12, exhibiting nearly identical behavior. Both signals were recorded through an audio interface and display Gibbs ringing [18], likely due to the input or decimation filters in the recording process [19][20].

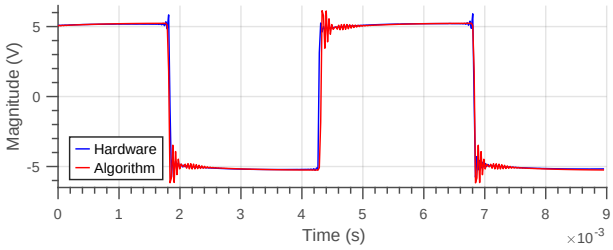

Figure 12: *Time domain analysis of square wave saturation with* 200Hz *Sine Source.* **Wave Shape** $= 5$.

The frequency locking behavior is fundamental to the functionality of the PLL. The behavior of PLL frequency locking is efficient and consistent with the hardware implementation across the mid-range frequency spectrum. Comparisons to the hardware effect are shown in fig. 13, with strong correlation between amplitude peaks between implementations. The behavior of the decade counter in the multiplier configuration has a strong effect on timbre and PLL system behavior, which has been replicated in the algorithm. This can be seen via inspection of the frequency response, with the highest amplitude placed at a lower frequency than the dotted line marking the expected multiplied frequency in both hardware and software. There is deviation in the hardware and software implementations respective to the magnitude of certain harmonics, this may be caused by op-amp clipping in the output stage and could be investigated further in future work.

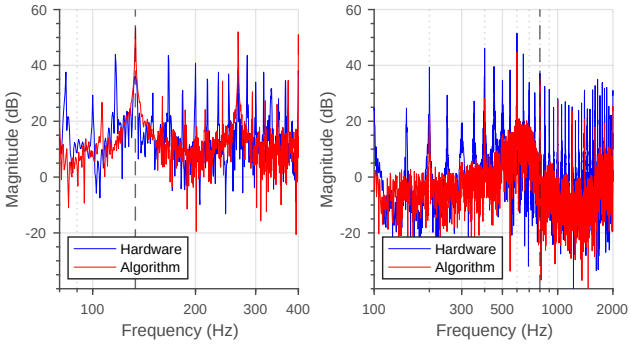

Figure 13: *PLL Frequency multiplication and division behavior.* **Multiplier** $= 4$, **Divider** $= 6$, *frequency targets marked by dotted line.*

The operation of the PLL is dependent on the behavior of the Loop Filter [12] and multiplier counter [13]. The effective execution of these behaviors is crucial in the achievement of phase locking in the circuit. The output of the PFD output may be observed

in fig. 14 under slow frequency locking conditions. The decay in pulse frequency over time with a constant frequency input demonstrates the successful frequency locking of the PLL model.

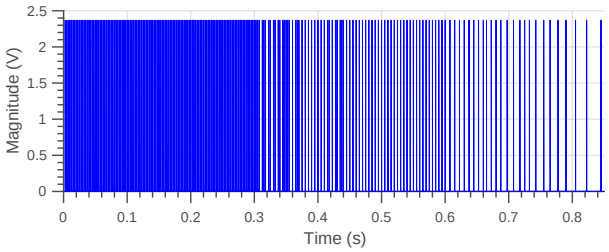

Figure 14: *PFD locked state pulses with sinusoidal input.*

The perceptual comparison of the digital implementation and the hardware effect is necessary in a complex system where some features may be unaccounted for in harmonic and time domain analysis. Use case audio samples from the algorithm and hardware are available in the accompanying GitHub repository[2]. In both 48 kHz and 192 kHz sampling rates, the algorithm is effective in comparison to the physical pedal. The lowest similarity of the signals is found in the frequency multiplied signal, where the digital model seems to have a longer response time than the hardware.

7. CONCLUSIONS AND FUTURE WORK

In this work, an analysis of the Schumann Electronics PLL and approach to modeling the mixed signal system was presented. State space matrices were utilized to simulate linear input amplification and filtering in the effect, while digital logic algorithms were developed from the behavior of CMOS logic integrated circuits in the effect. These algorithms were configured according to the pedal schematic and a full implementation in MATLAB was developed. The output from the algorithm was analyzed and displayed sufficient similarity in behavior to the hardware effect.

As this is a novel attempt to model a lesser-known guitar effect, there are still possible improvements to be made upon the methods presented. A more sophisticated model of the VCO stage of the PLL may be worthwhile, although its computational requirement may outweigh tonal advantages. A robust approach to reduce aliasing other than oversampling may also be applied, however difficulties may arise due to the nature of the conditional logic algorithms utilized for signal generation.

Other circuits may also be modeled using the methodologies presented in this paper—most readily, other PLL-based effects such as the Buchla 232 [21] frequency detector and Doepfer a-196 [22]. Opportunities for the utilization of these methods also lay outside of the scope of hardware simulation—primarily for the use of digital logic design concepts in one-bit music signals.

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